What is claimed is:

1. A semiconductor chip package comprising:

a semiconductor chip having signal electrode pads, ground electrode pads, and on-chip circuits, with said signal electrode pads for carrying electrical signals to and from the semiconductor chip, and said ground electrode pads for carrying ground and power signals;

a first dielectric layer overlying the chip and exposing the signal and the ground electrode pads;

a first metal layer formed on the first dielectric layer, the first metal layer including a ground metal layer in electrical communication with the ground electrode pads, said first metal layer comprising a plate structure;

a second dielectric layer formed on the first metal layer, the second dielectric layer having a ground contact opening therethrough and a signal contact opening therethrough; and

a second metal layer formed on the second dielectric layer, the second metal layer having ground and signal patterns, said ground patterns electrically connected to the ground electrode pads via the ground contact opening, and said signal patterns electrically connected to the signal electrode pads via the signal contact opening.

2. The semiconductor chip package of claim 1, wherein the ground metal layer comprises two metal plates symmetrically disposed about the electrode pads.

3. The semiconductor chip package of claim 1, wherein the ground metal layer includes an opening for exposing the electrode pads.

4. The semiconductor chip package of claim 1, further comprising external connections electrically connected to the ground and the signal patterns of the second metal layer.

5. The semiconductor chip package of claim 4, wherein the external connections are solder balls.

6. The semiconductor chip package of claim 1, wherein the first metal layer includes a contact pattern connected to the signal electrode pads.

7. The semiconductor chip package of claim 1, wherein the first and the second metal layer comprise copper.

8. The semiconductor chip package of claim 1, wherein the metal layers, the metal patterns and the dielectric layers are formed in the same batch process used for fabricating the on-chip circuits.

9. The semiconductor chip package of claim 1, further comprising a third dielectric layer, a third metal layer, a fourth dielectric layer and a fourth metal layer corresponding to the first dielectric layer, the first metal layer, the second dielectric layer and the second metal layer, respectively, overlying the semiconductor chip including the second metal layer.

10. The semiconductor chip package of claim 9, wherein the ground metal layer comprises two metal plates symmetrically disposed about the electrode pads.

11. The semiconductor chip package of claim 9, wherein the ground metal layer includes an opening for exposing the electrode pads.

12. The semiconductor chip package of claim 11, wherein the ground metal layer further comprises a plurality of through holes for connecting the first and the second dielectric layers.

13. The semiconductor chip package of claim 9, wherein the external connections are solder balls.

14. The semiconductor chip package of claim 9, wherein the first metal layer includes a contact pattern connected to the signal electrode pads.

15. The semiconductor chip package of claim 9, wherein the first and the second metal layer comprises copper.

16. The semiconductor chip package of claim 15, wherein the first metal layer is formed by sequentially stacking a titanium metal layer, a copper metal layer and a titanium metal layer.

17. The semiconductor chip package of claim 15, wherein the second metal layer is formed by sequentially stacking a chromium metal layer, a copper metal layer, a nickel metal layer.

18. The semiconductor chip package of claim 9, wherein the metal layers, the metal patterns and the dielectric layers are formed in the same batch process used for fabricating the on-chip circuits.

19. A semiconductor chip package comprising:
a semiconductor chip having electrode pads;
a first dielectric layer overlying the chip;
a first metal layer formed on the first dielectric layer;
a second dielectric layer formed on the first metal layer; and
a second metal layer formed on the second dielectric layer,
wherein one of the first and second metal layers comprises a ground metal layer having a plate structure.

20. The semiconductor chip package of claim 19, wherein the ground metal layer comprises two metal plates symmetrically disposed about the electrode pads.